XBox 360 Hardware Debug

Revision: 1.1

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Proprietary Notice

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Contents

Figures & Oscilloscope Captures

Revision History

Revision	*Date*	*Description*	*Revised by*
1	7/29/2005	• Initial document; credited documents Error.doc Xbox 360 Firmware Requirements..doc	a-garyf
1.1	8/8/2005	• Added/corrected sections	a-garyf
		•	
		•	

To-Do:

-add symptom>repair actions

-create flow chart

-get approval/recommendations on SRAs

-x-ray, boundary scan tests,

-add info on ways to trick the SMC to not see error status, use old kernel,

Reference Documents

Microsoft Specifications Documents

Errors.doc

XBox 360 Firmware Requirements.doc

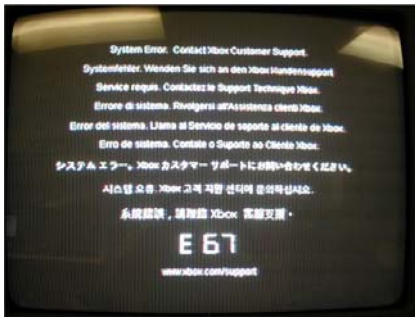
POR Diagram

Component Data Sheets

1 Error Codes

The following sections will quickly allow the *technician* to identify error codes from the video screen or front panel LED display. The resulting error codes can be used by troubleshooters to easily determine what core system component is failing, and narrow down possible recovery options. All error codes displayed in this list are consistent across all iterations of the console design. Refer to MSDTBD2 for error code display mapping for additional codes that may vary depending on the console design.

1.1 Video Screen UEM Error Codes



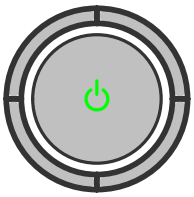
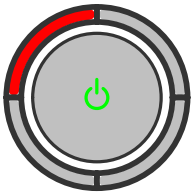
UEM Error Codes are displayed on the screen as well as on the front panel LED display.

The decimal number displayed on screen can be used to look up error code details and repair actions. See table #XSS-Detected Error List for troubleshooting and repair actions.

In the example on the left, the decimal number 67 can be identified from the error list tables as an error related to the Hard Drive Timing out.

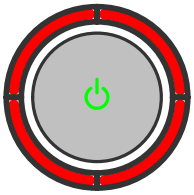
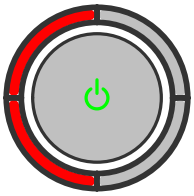
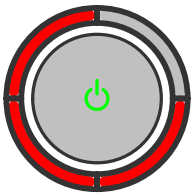
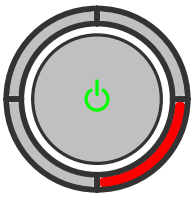
1.2 Front Panel Normal Mode

Table 1 Normal Mode

Normal Mode	LED Display
Powered Up and No Controller Connected	
Powered Up and Controller Connected	

1.3 Front Panel Failure Mode

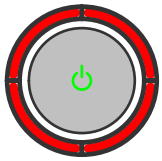
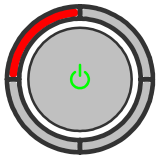
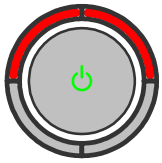
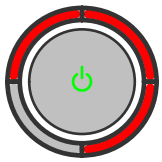
Table 2 Failure Mode

Failure mode	LED Display (Red indicates Flashing)
AV Cable not connected to console	
Thermal Overload	
Core Digital or System Component Failure	
Universal Error Message on screen	

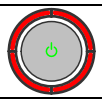
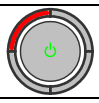
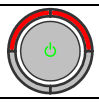
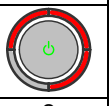
1.4 Error Code Identification

General failure modes are shown above in Table 1. When a general failure mode is displayed it is possible to further view an error code on the front panel LED display providing details as to the nature of the failure, hardware section, component failed, and repair actions. The error code is read two bits at a time most significant bits first to form a byte code value. This byte value is used to look up the error code details in the SMC & XSS Detected Error Lists and Repair Actions.

- Holding the binding button while pressing the eject button once shall cause one of the following values to light up, based on the value of bits 7 and 6 of the error code.

Value	LED Display *(Red indicates Flashing)*
0	
1	
2	
3	

- Holding the binding button while pressing the eject button again shall cause one of the above values to light up, based on the value of bits 5&4 in a manner similar to bits 7&6.
- Holding the binding button while pressing the eject button two more times shall cause the values to light up with each press, corresponding to bits 3&2, then 1&0.
- Holding the binding button while pressing the eject button a fifth time shall cause the failure mode to be displayed again.
- Example retrieving the Error Code:

Bits	7& 6	5 & 4	3 & 2	1 & 0		
Displayed						
Value	0	1	2	3		
					Binary Value	Hex Error Code
Bit Value	00	01	10	11	00011011	1B

- Look up Error Code in the SMC-Detected Error List and XSS-Detected Error List.
- See section Component Level Troubleshooting & Repair for repair actions.

Error Code Identification Examples

A binary to hex conversion table is included in this document. Once the binary value is identified and converted to hex, look up the hex error code in the SMC-Detected Error List.

Table 3 Example: Error Code 0x03

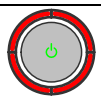
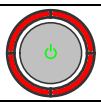
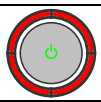
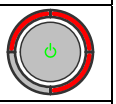
Bits	7& 6	5 & 4	3 & 2	1 & 0			
Displayed							
Value	0	0	0	3			
					Binary Value	Hex Error Code	SMC-Detected Error List
Bit Value	00	00	00	11	00000011	03	ERROR_V_GPUCORE

Table 4 Example: Error Code 0x14

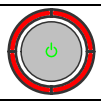
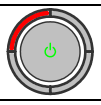
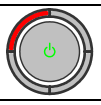
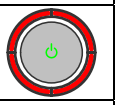
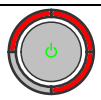
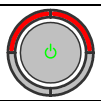
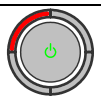
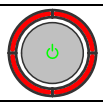
Bits	7& 6	5 & 4	3 & 2	1 & 0			
Displayed							
Value	0	1	1	0			
					Binary Value	Hex Error Code	SMC-Detected Error List
Bit Value	00	01	01	00	00010100	14	ERROR_MEMORY_ADDRESSING

Table 5 Example: Error Code 0xE4

Bits	7& 6	5 & 4	3 & 2	1 & 0			
Displayed							
Value	3	2	1	0			
					Binary Value	Hex Error Code	SMC-Detected Error List
Bit Value	11	10	01	00	11100100	E4	Elvis is Alive

1.5 SMC-Detected Error List

The SMC detects the following errors and shall behave as described in the error classes section. For up-to-date error codes refer Error.doc. **Error Codes with leading 0x are in HEX and values without are in decimal.**

[Note: The table below is link embedded to the source document Error.doc. Changes to Error.doc are reflected in the list. Changes to this document will not be permanently saved. \\Xenon\hwdev\Electrical\Architecture\Test\Error.doc]

Error Name	Precedence /Class	User Error Pattern	Error Bit	Error Code	Description
ERROR_V_12P0	EC_FATAL	E_SYSTEMCOMPONENT	0x01	0x01	ANA_V12P0_PWRGD was negated unexpectedly
ERROR_V_CPUCORE	EC_FATAL	E_SYSTEMCOMPONENT	0x02	0x02	VREG_CPU_PWRGD was negated unexpectedly
ERROR_V_GPUCORE	EC_FATAL	E_SYSTEMCOMPONENT	0x03	0x03	VREG_GPU_PWRGD was negated unexpectedly
ERROR_NO_ANA	EC_FATAL[1]	E_SYSTEMCOMPONENT	0x04	0x04	Ana is not responding to reads/writes
ERROR_THERMAL_CPU	EC_THERMAL	E_THERMAL	0x05	0x05	A thermal overload occurred in the CPU
ERROR_THERMAL_GPU	EC_THERMAL	E_THERMAL	0x06	0x06	A thermal overload occurred in the GPU
ERROR_THERMAL_EDRAM	EC_THERMAL	E_THERMAL	0x07	0x07	A thermal overload occurred in the EDRAM
ERROR_GPU_RST_DONE	EC_BOOT	E_SYSTEMCOMPONENT	0x08	0x08	GPU_RST_DONE was not asserted in time during seqUnReset
ERROR_NO_PCIE	EC_BOOT	E_SYSTEMCOMPONENT	0x9	0x9	The PCI-E link failed to enter L0 in time during seqUnReset
ERROR_NO_HANDSHAKE	EC_BOOT	E_SYSTEMCOMPONENT	0xA	0xA	The CPU failed to send GetPowerUpCause to the SMC. Also used for Titan retries.
ERROR_NO_CLOCKCHIP	EC_FATAL	E_SYSTEMCOMPONENT	0xB	0xB	Backup clock chip (ICS/Cypress) is not responding to reads or writes (only in Retail mode)
ERROR_NO_TEMPERATURES	EC_FATAL	E_SYSTEMCOMPONENT	0xC	0xC	Ana responds to temperature reads, but fails to provide temperature samples (registers read as zero).
RESERVED*Reserved*_0x0D_0x0F	*Reserved*	n/a	0xD-0xF	0xD-0xF	Not used

1.6 XSS-Detected Error List

The following errors are detected by XSS, and reported to the SMC. *For up-to-date error codes refer to Error.doc.* **Error Codes with leading 0x are in HEX and values without are in decimal.**

[Note: The table below is link embedded to the source document Error.doc. Changes to Error.doc are reflected in the list. Changes to this document will not be permanently saved. \\Xenon\hwdev\Electrical\Architecture\Test\Error.doc]

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[1] Note that Ana not responding is not strictly a voltage error, but the desired behavior is the same. If Ana cannot be reached, the SMC cannot monitor system temperature, and the console cannot be operated safely. In this case, the console should never be allowed to boot (if detected pre-boot), or should be shut down immediately upon detection.

2 Component Level Troubleshooting & Repair

This section covers possible repair actions associated with Error Codes listed in the SMC-Detected Error List and XSS-Detected Error List. As a troubleshooting aid a brief Architecture Notes sections is including covering the vital role of the System Management Controller (SMC) in power up sequencing and reset control.

2.1 Symptom>>Repair Action Quick Flow Chart

{Insert here}

2.2 Symptom ERROR_V_12P0

ERROR_V_12P0	EC_FATAL	E_SYSTEMCOMPONENT	0x01	0x01	ANA_V12P0_PWRGD was negated unexpectedly

Description

The power connector J9A1 connects to the external power supply. The external power supply supplies 5 DC volts (V_5P0STBY) and 12 DC volts (V_12P0). The standby voltage V_5P0STBY is used to supply the other standby converted voltages V_3P3STBY and V_1P8STBY. The SMC and Argon are powered by the standby voltages. When the SMC has detected that the user wishes to turn on the console (go from standby mode to full power) the SMC asserts the signal PSU_V12P0_EN to the external power supply. This signal tells the external power supply to turn on the 12volts (V_12P0). V_12P0 is the main voltage to the motherboard power controllers/regulators of the CPU, GPU, Memory, and other. ANA (U4B1) monitors V12P0 for correct tolerance. Out of tolerance conditions are indicated by ANA on signal ANA_V12P0_PWERGD pin 122. 12V tolerance & trip points are set with resistors R4B9, R4B8, R4B2 on ANA pin V_12P0_DET.After the SMC asserts PSU_V12P0_EN it waits xx ms for the power good signal ANA_V12P0_PWERGD. If it does not detect power good it will de-asserts the enable line and display ERROR_V_12P0 on the front panel.

Possible Repair Actions

Check using a known good external power supply.

Check for shorts on power sections and in particular V_12P0 and the standby voltages –see #Voltage Resistance List.

Check PSU_V12P0_EN and ANA_V12P0_PWERGD trace and resistor circuits

Detailed Troubleshooting Options

Check V_12P0_DET circuit –see pin U4B1 pin 112

Check for shorts/opens/missing components/wrong values on the following: PSU_V12P0_EN, ANA_V12P0_PWERGD, ANA (U4B1) pin names V_12P0_OK, V_12P0_DET, VAA_POR18S, AVSS_POR18S, VAA_POR33S, AVSS_POR33S, components R8A2; R8A1, R4B9, R4B8, R4B2

Check R8A2.

It can be helpful to load an early version of SMC/Kernel build 1800 firmware or earlier in which SMC did not monitor the power status lines such as ANA_V12P0_PWERGD. This way the SMC will not de-assert the signals that enable the power controllers/regulators.

2.3 Symptom ERROR_V_CPUCORE

ERROR_V_CPUCORE	EC_FATAL	E_SYSTEMCOMPONENT	0x02	0x02	VREG_CPU_PWRGD was negated unexpectedly

Description

On power on the SMC enables the 5V power controller U4V1 with signal VREG_V5P0_EN then enables CPU power controller U7U1 with signal VREG_CPU_EN. The CPU power controller indicates power status on the signal VREG_CPU_PWRGD. This signal is monitored by the SMC. This signal should go high indicating good power. If the SMC fails to detect good power it disables the power controllers and displays the above error code. It is important to note that V_5P0 is the pull-up voltage used on the CPU circuit signal VREG_CPU_PWRGD. If VREG_CPU_PWRGD does not go high it can be a problem with either U7U1 (V_CPUCORE) or U4V1 (V_5P0) circuits. Using V_5P0 as a pull-up voltage for the CPU circuit is a means to monitor good status on both power circuits.

Possible Repair Actions

Check for shorts and proper voltages on V_CPUCORE and V5P0 –see #Voltage Resistance List

Check for missing components or incorrect values within the CPU Power Controller section.

Check for missing components or incorrect values within the V5P0 Power Controller section.

Replace U7U1

Replace U4V1

Detailed Troubleshooting Options

Check pull-up/pull-down resistors and traces on power controller's enable and status signals. Note: VREG_CPU_PWRGD uses the V_5P0 as the pull-up voltage.

Check: Using a storage scope check VREG_V5P0_EN to V5P0 and VREG_CPU_EN to V_CPUCORE, and VREG_CPU_PWRGD.

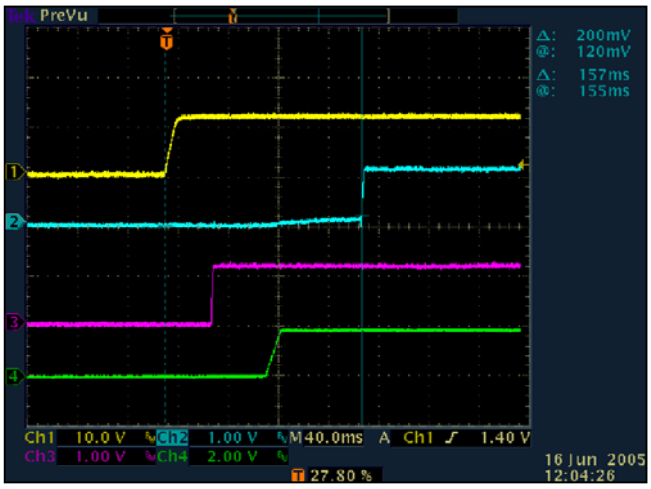
You can often get closer to the source of the problem using the table example below. Remove the power cord to the console; compare resistances values on the pins of U7U1/ U4V1 to that of a good board. Or in standby mode compare voltages.

Table 6 U7U1 Reference Measurements

U7U1 KNOWN GOOD VALUES					
pin	Resistance	Voltage	pin	Resistance	Voltage
1			15		
2			16		
3			17		
4			18		
5			19		
6			20		
7			21		
8			22		
9			23		
10			24		
11			25		
12			26		
13			27		
14			28		

U7U1 UNDER REPAIR					
pin	Resistance	Voltage	pin	Resistance	Voltage
1			15		
2			16		
3			17		
4			18		
5			19		
6			20		
7			21		
8			22		
9			23		
10			24		
11			25		
12			26		
13			27		
14			28		

+12V Rise to

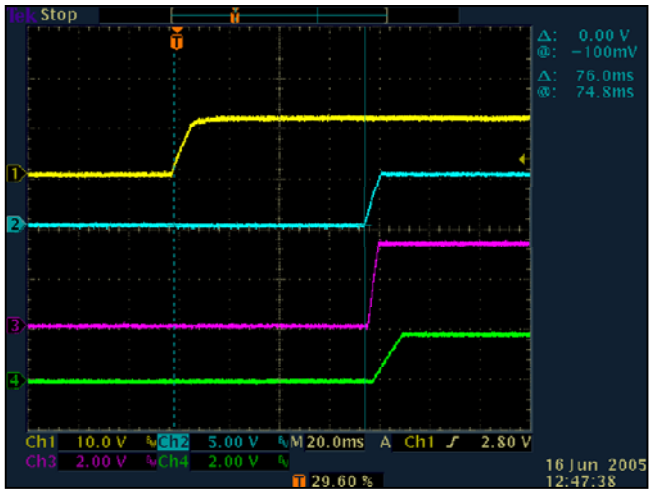


CH1: +12V

CH2: **V_CPUCORE (157ms)**

CH3: V_GPUCORE (36.8ms)

CH4: V_MEM (80ms)



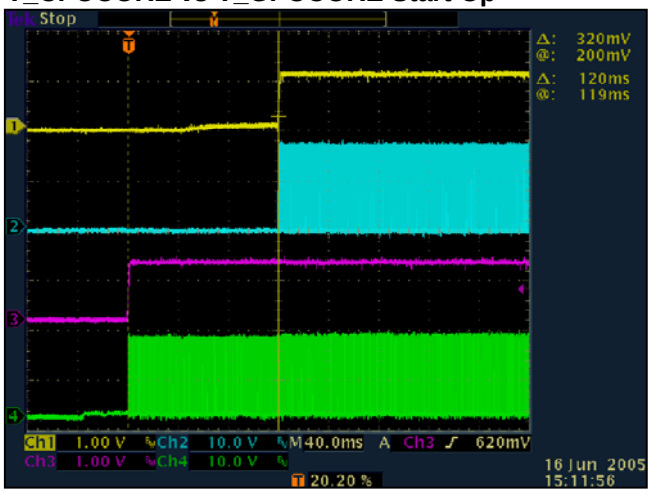
CH1: +12V

CH2: **V_5P0 (76ms)**

CH3: V_3P3 (76ms)

CH4: V_MEM (80ms)

V_CPUCORE vs V_GPUCORE Start-Up



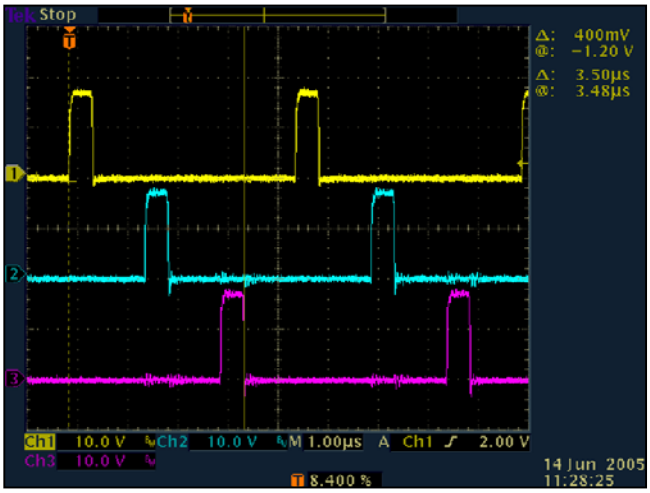
CH1: V_CPUCORE

CH2: CPU High-Side FET Gate

CH3: V_GPUCORE

CH4: GPU High-Side FET Gate

V_CPUCORE 3-Phase Timing

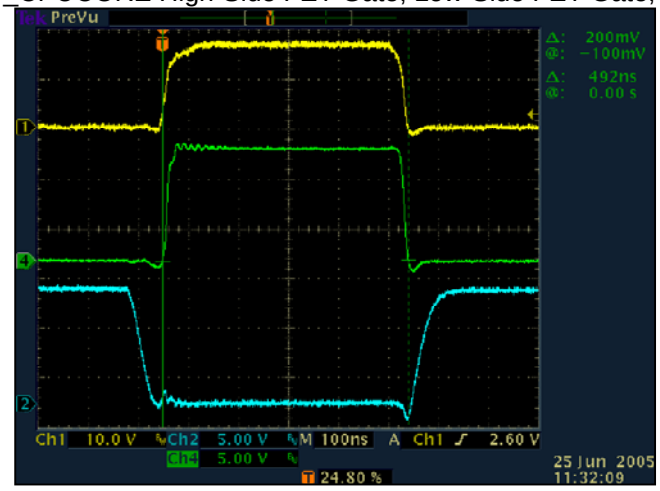


CH1: V_CPUCORE Phase 1

CH2: V_CPUCORE Phase 2

CH3: V_CPUCORE Phase 3

V_CPUCORE High-Side FET Gate, Low-Side FET Gate, and Vreg_CPU_Phase 1



CH1: VREG_CPU_GH1

CH4: VREG_CPU_PHASE 1

CH2: VREG_CPU_GL1

2.4 Symptom ERROR_V_GPUCORE

ERROR_V_GPUCORE	EC_FATAL	E_SYSTEMCOMPONENT	0x03	0x03	VREG_GPU_PWRGD was negated unexpectedly

Description

On power on the SMC enables the GPU power controller U8N1 with signal VREG_GPU_EN_N. The power controller indicates power status on the signal VREG_GPU_PWRGD. This signal is monitored by the SMC. This signal should go high indicating good power. If the SMC fails to detect good power it disables the power controller and displays the above error code

Possible Repair Actions

Check for shorts and proper voltage on V_GPUCORE –see #Voltage Resistance List

Check signal from the GPU regulator U8N1 to the SMC R8N17 & R8N18.

Check for missing components or incorrect values within the GPU Power Controller section.

Replace U8N1

Detailed Troubleshooting Options

You can often get closer to the source of the problem using the table example below. Remove the power cord to the console; compare resistances values on the pins of U8N1 to that of a good board. Or in standby mode compare voltages.

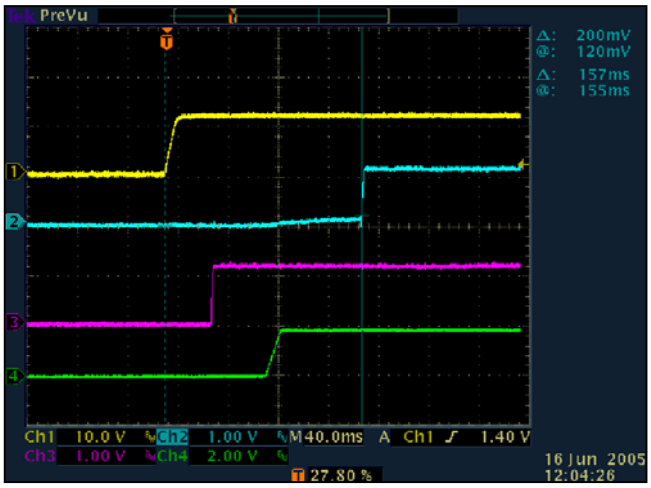
Table 7 U8N1 Reference Measurements

U8N1 KNOWN GOOD VALUES					
pin	Resistance	Voltage	pin	Resistance	Voltage
1			17		
2			18		
3			19		
4			20		
5			21		
6			22		
7			23		
8			24		
9			25		
10			26		
11			27		
12			28		
13			29		
14			30		
15			31		
16			32		

U8N1 UNDER REPAIR					
pin	Resistance	Voltage	pin	Resistance	Voltage
1			17		
2			18		
3			19		
4			20		
5			21		
6			22		
7			23		
8			24		
9			25		
10			26		
11			27		
12			28		
13			29		
14			30		
15			31		
16			32		

Oscilloscope Captures

+12V Rise to



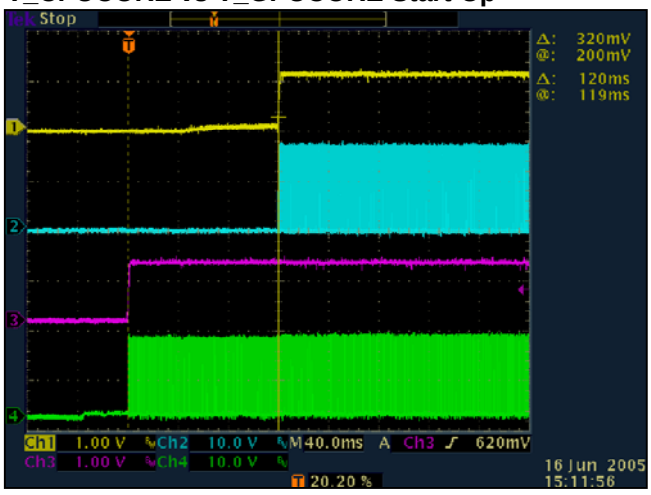
CH1: +12V

CH2: V_CPUCORE (157ms)

CH3: **V_GPUCORE (36.8ms)**

CH4: V_MEM (80ms)

V_CPUCORE vs V_GPUCORE Start-Up



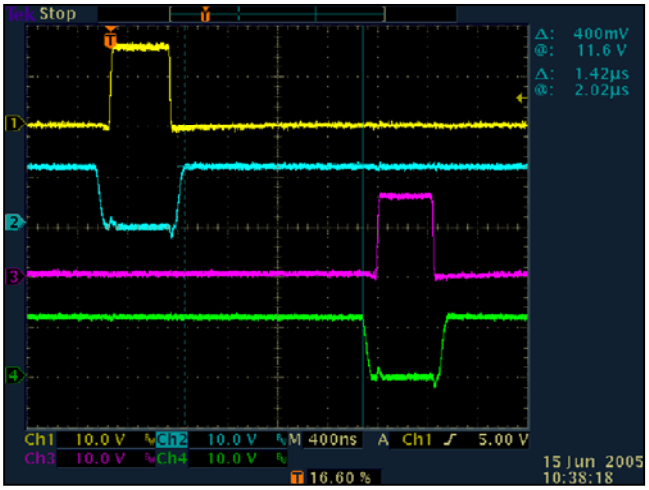
CH1: V_CPUCORE

CH2: CPU High-Side FET Gate

CH3: V_GPUCORE

CH4: GPU High-Side FET Gate

1.3 V_GPUCORE Phase 1 / Phase 2 Timing



CH1: Phase 1 High-Side FET Gate

CH2: Phase 1 Low-Side FET Gate

CH3: Phase 2 High-Side FET Gate

CH4: Phase 2 Low-Side FET Gate

2.5 Symptom ERROR_NO_PCIE

Description

Possible Repair Actions

Check for shorts and proper voltage on V_GPUPCIE –see #Voltage Resistance List

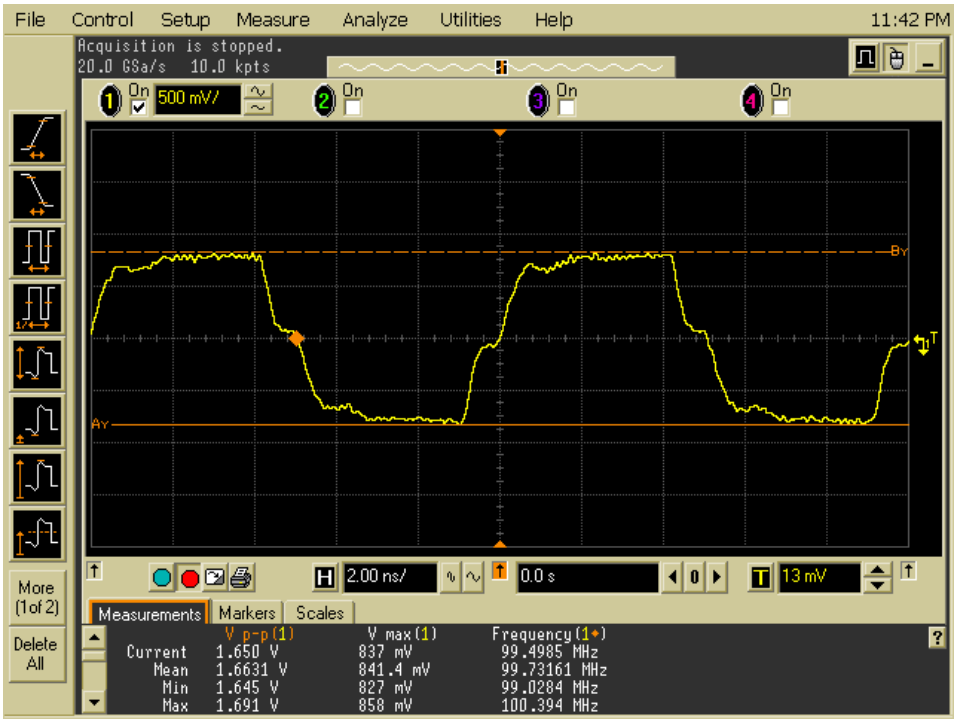
Replace U5C1 if V_GPUPCIE voltage bad

Check for shorts and proper voltage on V_SBPCIE –see #Voltage Resistance List

Replace U3P1 if V_SBPCIE voltage bad

Detailed Troubleshooting Options

Check clock PCIEX_CLK_DP/DN and GPU_CLK_DP/DN



Check for shorts/opens or resistance differences between the PCIE signals below. The signals all should equal. Check in series resistors if difference.

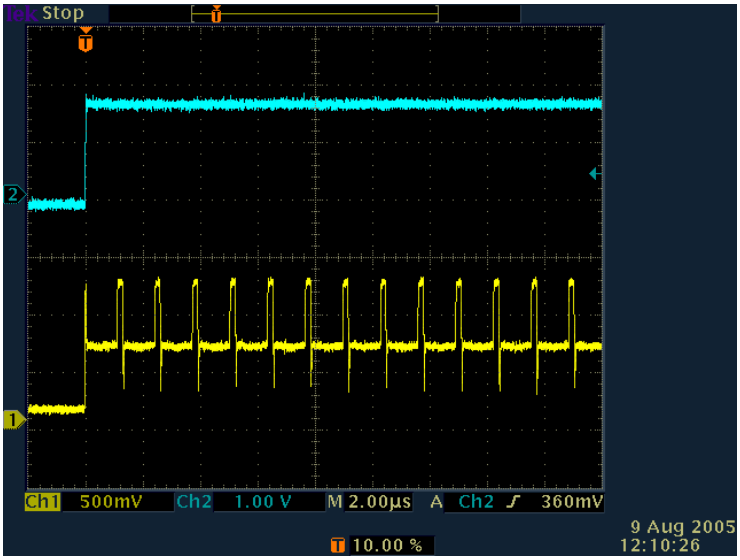
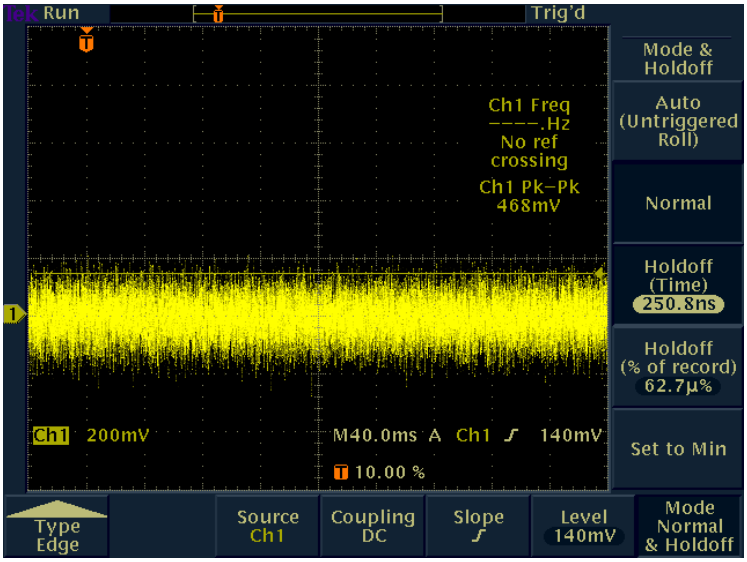
PEX_GPU_SB_L0_DP resistance =
PEX_GPU_SB_L0_DN resistance =
PEX_GPU_SB_L1_DP resistance =
PEX_GPU_SB_L1_DN resistance =
PEX_SB_GPU_L0_DP resistance =
PEX_SB_GPU_L0_DN resistance =
PEX_SB_GPU_L1_DP resistance =
PEX_SB_GPU_L1_DN resistance =

Check PCIE power to SB pins through inductors FB2P2 and resistor R2P17

Check calibration circuits GPU pins PEX_PCAL, PEX_NCAL, PEX_ICAL

Check calibration circuits SB pins PEX_RBIAS0, PEX_RBIAS1

Oscilloscope Captures

	GPU_RST_DONE_N PEX_GPU_SB_L1_DN
	

2.6 Symptom ERROR_NO_HANDSHAKE

Description

At this point of failure the V_CPUCORE is good, the PCI-E link has entered into a known good state, and the SMC releases the CPU reset line CPU_RST_N. CPU_RST_N is expected to go high. The SMC monitors the CPU initialization process as it comes out of reset and begins to execute code. If the CPU fails to initialize properly the SMC will enter the error state ERROR_NO_HANDSHAKE.

Possible Repair Actions

Check CPU power & resistances:

X801054-007

Signal Name	Impedance Expected Result	min		nom		max	
V_CPUCORE	>4 ohms	1	V	1.145	V	1.275	V
V_CPUPLL	K ohms	2.09	V	2.2	V	2.31	V
V_1P8	>100 ohms	1.748	V	1.8	V	1.851	V

Check CPU connectivity to board using Manufacturing JTAG boundary scan tests

Detailed Troubleshooting Options

Check CPU_RST_N,

Check CPU Clock

Figure 1 CPU Clock R3C17 & R3C18

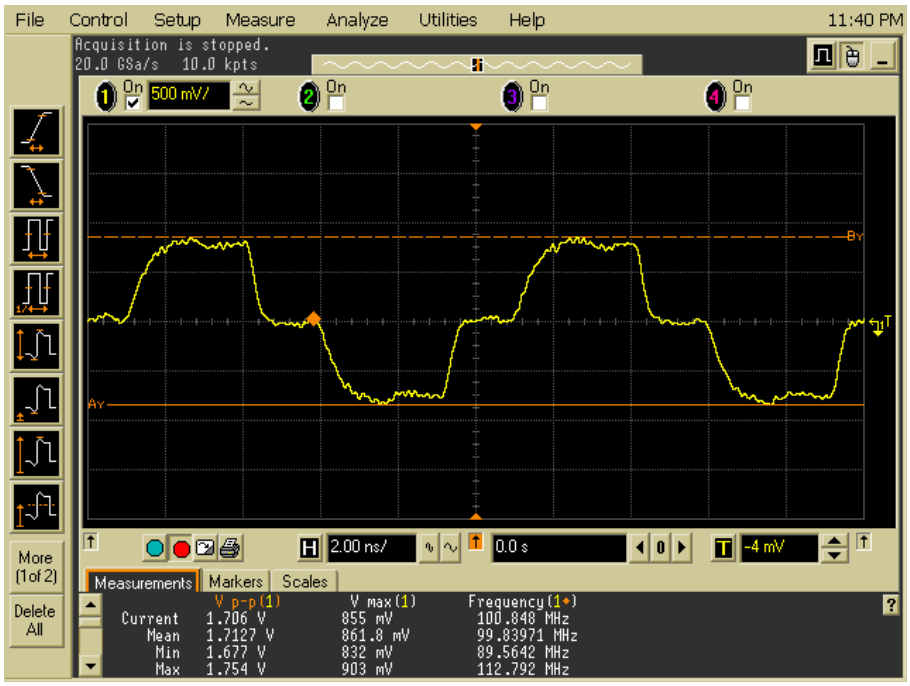


Figure *2 Example 2*

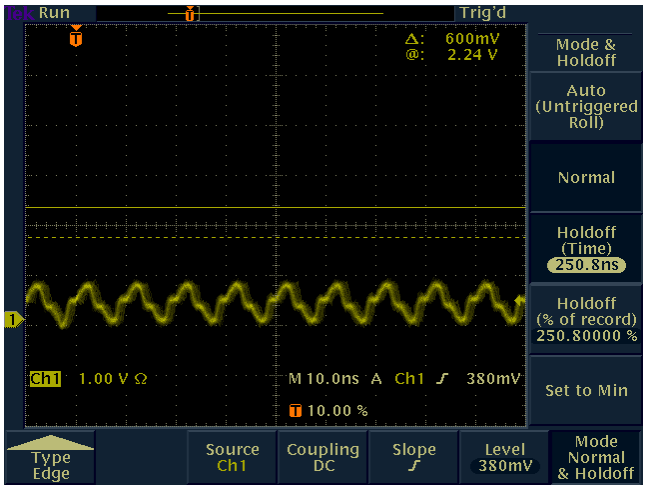
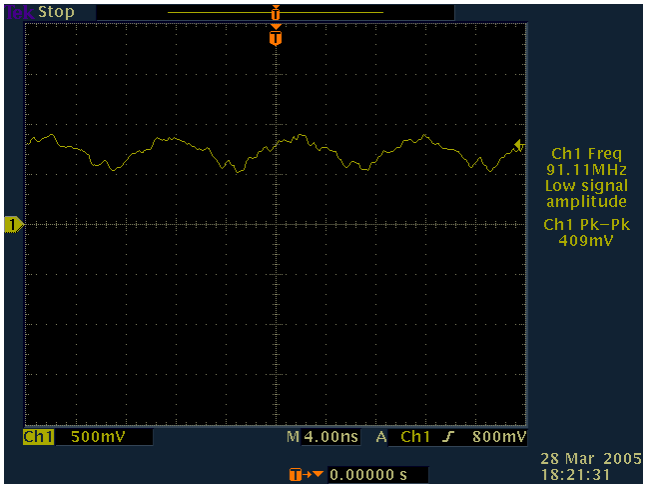


Figure 3 Bad CPU Clock Example



Check that CPU gets released from Reset.

Board Ref	*Signal*	*Standby Mode*	*Running Mode*	*Signal Location*
X801054-007	*CPU_RST_V1P1_N*	*0 volts*	*>1 volt*	*J8C1 PIN 2*

Check JTAG signals

Do a visual of the board looking for:

- Missing components
- Wrong components installed; for example capacitor in resistor location.
- Wrong values installed

2.7 Symptom ERROR_NBINIT_MEM_VENDOR_ID

Description

Memory device vendor ID read failed or mismatch between devices

Possible Repair Actions

Run manufacturing boundary scan tests.

Run GDDRQual tests

Check V_MEM voltage #Voltage Resistance List

Try new latest Kernel firmware

Detailed Troubleshooting Options

HyperTerminal: Open HyperTerminal using the appropriate com port connected to the Lamprey with settings 115200; 8 Data Bits; Parity None; 1 Stop Bits; Flow control none. Be sure you have selected *CALL* from the HyperTerminal window option to connect. Power on the console and check for screen output to HyperTerminal.

2.8 Symptom ERROR_NBINIT_MEM_READ_STROBE_DATA_WRITE

Description

Possible Repair Actions

Run manufacturing boundary scan tests.

Run GDDRQual tests

Check V_MEM voltage #Voltage Resistance List

Try new latest Kernel firmware

Detailed Troubleshooting Options

HyperTerminal: Open HyperTerminal using the appropriate com port connected to the Lamprey with settings 115200; 8 Data Bits; Parity None; 1 Stop Bits; Flow control none. Be sure you have selected *CALL* from the HyperTerminal window option to connect. Power on the console and check for screen output to HyperTerminal.

2.9 Symptom ERROR_NBINIT_MEM_READ_STROBE_DELAY_TRAINING

Description

Memory read strobe delay training failed

Possible Repair Actions

Run manufacturing boundary scan tests.

Run GDDRQual tests

Check V_MEM voltage #Voltage Resistance List

Try new latest Kernel firmware

Detailed Troubleshooting Options

HyperTerminal: Open HyperTerminal using the appropriate com port connected to the Lamprey with settings 115200; 8 Data Bits; Parity None; 1 Stop Bits; Flow control none. Be sure you have selected

CALL from the HyperTerminal window option to connect. Power on the console and check for screen output to HyperTerminal.

2.10 Symptom ERROR_NBINIT_MEM_WRITE_STROBE_DELAY_TRAINING

Description

Memory write strobe delay training failed

Possible Repair Actions

Run manufacturing boundary scan tests.

Run GDDRQual tests

Check V_MEM voltage #Voltage Resistance List

Try new latest Kernel firmware

Detailed Troubleshooting Options

HyperTerminal: Open HyperTerminal using the appropriate com port connected to the Lamprey with settings 115200; 8 Data Bits; Parity None; 1 Stop Bits; Flow control none. Be sure you have selected *CALL* from the HyperTerminal window option to connect. Power on the console and check for screen output to HyperTerminal.

2.11 Symptom ERROR_MEMORY_ADDRESSING

Description

Memory address line failure

Possible Repair Actions

Run manufacturing boundary scan tests.

Run GDDRQual tests including script CheckAddress2.txt

Check V_MEM voltage #Voltage Resistance List

Try new latest Kernel firmware

Detailed Troubleshooting Options

HyperTerminal: Open HyperTerminal using the appropriate com port connected to the Lamprey with settings 115200; 8 Data Bits; Parity None; 1 Stop Bits; Flow control none. Be sure you have selected *CALL* from the HyperTerminal window option to connect. Power on the console and check for screen output to HyperTerminal.

2.12 Symptom ERROR_MEMORY_DATA

Description

Memory data line failure

Possible Repair Actions

Run manufacturing boundary scan tests.

Run GDDRQual tests including script CheckData.txt

Check V_MEM voltage #Voltage Resistance List

Try new latest Kernel firmware

Detailed Troubleshooting Options

HyperTerminal: Open HyperTerminal using the appropriate com port connected to the Lamprey with settings 115200; 8 Data Bits; Parity None; 1 Stop Bits; Flow control none. Be sure you have selected *CALL* from the HyperTerminal window option to connect. Power on the console and check for screen output to HyperTerminal.

2.13 Symptom [*please use this Symptom>Repair Action format*]

Description

Possible Repair Actions

Detailed Troubleshooting Options

Oscilloscope Captures

3 Symptom DIED DIED BOARD ISSUES

3.1 Standby Voltages

3.1.1 V_3P3STBY, V_1P8STBY, V_5P0STBY, and V_5P0DUAL

Description

The power connector J9A1 connects to the external power supply. The external power supply supplies 5 DC volts (V_5P0STBY) and 12 DC volts (V_12P0). The standby voltage V_5P0STBY is used to supply the other standby converted voltages V_3P3STBY and V_1P8STBY. When the power cord is installed into the motherboard J9A1 connector V_5P0STBY from the external power supply is immediately feed into the V_3P3STBY and V_1P8STBY regulators. There is no enable or disable feature of these regulators and no enable or disable of V_5P0STBY. The standby voltages are vital to the operation of the SMC. The SMC is a microcontroller located in the Xenon Southbridge. It controls the power up sequencing and functions. See Architecture Notes section for greater details on the vital role the SMC plays in the power up sequencing and reset control. Without proper standby voltages the board is died died. Special Note: ANA (U4B1) monitors V_3P3STBY and V_1P8STBY for proper tolerance. If either voltage is out of tolerance ANA will hold the SMC in reset with signal SMC_RST_N.

Possible Repair Actions

The following voltages tolerances are referenced in #Voltage Resistance List

V_5P0STBY voltage issue:

- check using a known good external power supply
- check for short and proper voltage on V_5P0STBY see
- check V_5P0DUAL circuit and bleeder circuit.

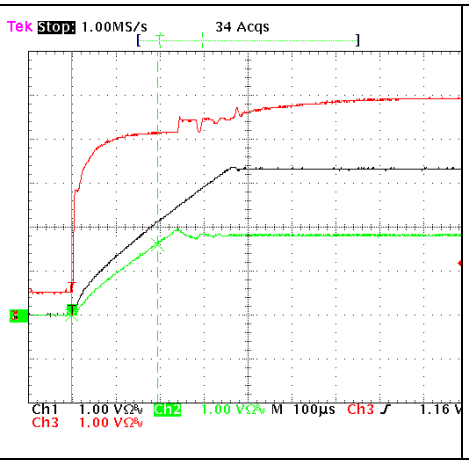
V_3P3STBY voltage issue:

- check for proper V_5P0STBY voltage on input to U5B1 (V_3P3STBY) regulator
- check for short on V_3P3STBY see #Voltage Resistance List
- replace U5B1

V_1P8STBY voltage issue:

- check for proper V_5P0STBY voltage on input to U5B2 (V_1P8STBY) regulator
- check for short on V_1P8STBY see #Voltage Resistance List
- replace U5B2

Oscilloscope Captures



Ch1 = V_3P3STBY

Ch2 = V_1P8STBY

Ch3 = V_5P0STBY

Plug PSU into wall first, and then plug into motherboard.

Standard board…Fab B.

3.2 Died SMC

3.2.1 SMC Code

{Quick reprogramming}

3.2.2 SMC_RST_N

Description

ANA (U4B1) monitors V_3P3STBY and V_1P8STBY for proper tolerance. If either voltage is out of tolerance ANA will hold the SMC in reset with signal SMC_RST_N.

Possible Repair Actions

Check for proper Standby Voltages in the Standby Voltages section.

Detailed Troubleshooting Options

Check for proper SMC_RST_N signal

- Short or open on SMC_RST_N
- R2P1, R2P3 values
- Bleeder circuit R1V1, Q1V1, etc…
- ANA power and GND signals VAA_POR18S, AVSS_POR18S, VAA_POR33S, AVSS_POR33S

3.3 Symptom [*please use this Symptom>Repair Action format*]

Description

Possible Repair Actions

Detailed Troubleshooting Options

Oscilloscope Captures

4 KD Output Hangs & Errors

4.1 Symptom LOAD_DRIVERS, LOAD_XAM, XAM.XEX FAILED TO START

Description

Consistent console errors/hangs after modules LOAD_DRIVERS or LOAD_XAM are often the result of mismatched or corrupted kernel and file systems builds programmed into flash memory. This may occur during incomplete recoveries and user errors. If your console boots past these modules sometimes then it is not a mismatch or corrupted kernel and file system and more likely another problem.

Possible Repair Actions

1. Check that there is no CD in the console (Be sure no recovery CD in installed)
2. Program the kernel to flash with a known good build.
3. Program the file system to flash using the *matching* build number.
4. Power on the console with KD running and check boot status.
5. Video output may not be present until a recovery is completed.

Running Recovery: Run a network recovery or CD recover using the *same build used for the kernel and file system*.

- Do not run a network recovery while any recovery CD is installed in the CDROM drive.

5 NO KD Output

5.1 Symptom No KD Output

Description

Possible Repair Actions

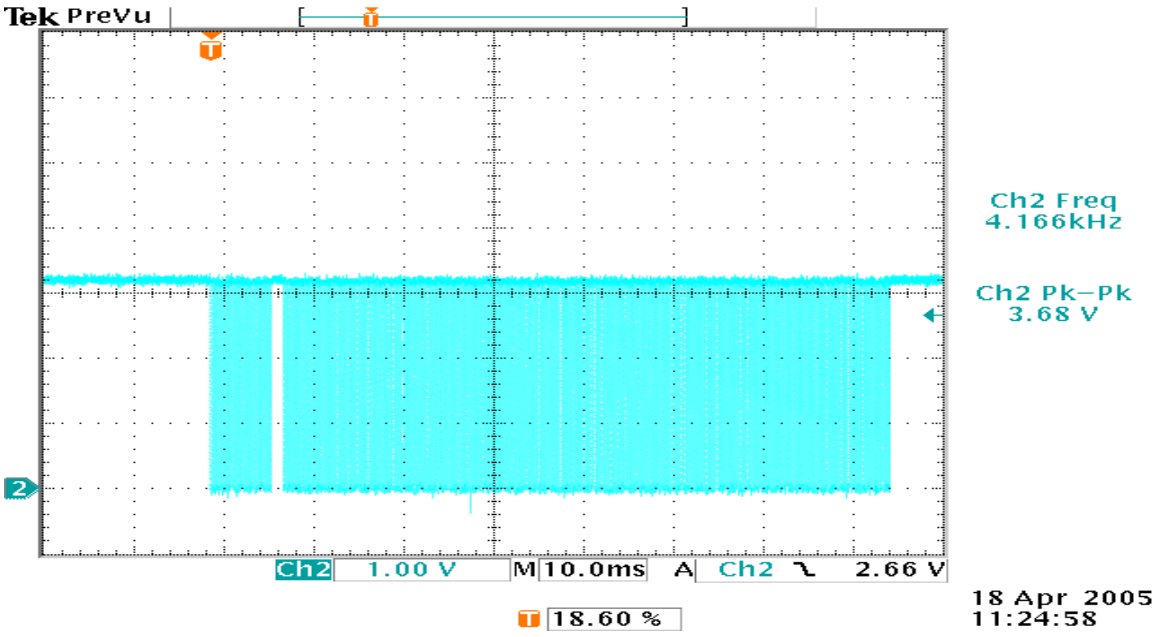
- Check front panel LED for error status. Be sure your Argon is working with up-to-date firmware.
- Close the KD window

- Open HyperTerminal using the appropriate com port connected to the Lamprey with settings 115200; 8 Data Bits; Parity None; 1 Stop Bits; Flow control none. Be sure you have selected *CALL* from the HyperTerminal window option to connect.
- Power on the console and check for screen output to HyperTerminal. If no output to HyperTerminal check:
    a. Check your HyperTerminal connection and configuration by connecting a known good console
- If you know that your HyperTerminal configuration is working but you get no screen output:
    a. Check that the fans are turning on.
    b. Check for the heartbeat signal.
    c. Check the voltages on the motherboard –see Board Voltages.
    d. Try reprogramming the kernel to flash.
    e. Check that the BSB LED is on.
    f. Quick Check that the flash chip-select signal is active during power up from the pad of R1E2 trace leading to the Flash U2E1.

Detailed Troubleshooting Options

If the CPU is not accessing flash during power-on their will no activity on FLSH_CE as shown in Figure below.

Figure 4 Good FLSH_CE During Power On



6 Architecture Notes

6.1 SMC

The System Management Controller (SMC) is a microcontroller located in the Xenon Southbridge. It provides reliable and robust system control functions. The SMC is always powered from the regulators fed by the standby rail in Xenon's external power supply brick. It communicates with the system CPU via the System Management Module (SMM). This interface is described in *XBox 360 Southbridge System Management Module (SMM) Design Specification*. The SMC detects many of the errors explained in this document and the SMC shall behave as described in the error classes section below.

6.2 SMC Duties

A few of the duties of the SMC include the following

- System power supply and voltage regulator control
- System reset and clock control
- Audio clamp control
- XSS access to the hardware real time clock (RTC)
- Decode Infrared (IR) remote protocol
- Temperature monitoring and fan control
- Front panel IO (power, eject and binding buttons)
- Console orientation detection (tilt switch)
- Communication with Front Panel Module (NV storage, LEDs)
- Audio/Video Interface Port (AVIP) monitoring
- Control of and access to system I2C Bus
- Control of and access to AV Pack I2C Bus
- Optical Disk Drive (ODD) tray control
- Southbridge PCI Express PLL programming
- Rudimentary system tests and diagnostics

6.3 Power Up Sequence

This section is included only for general purpose understanding and may not be accurate. Please refer to the Error.doc, XBox 360 Firmware Requirements.doc, and POR Diagram for complete and accurate descriptions.

SMC controls powering up the console. See also the SMC section.

- After ANA_V12P0_PWRGD is detected[2], or after tPSU has expired past asserting PSU_V12P0_EN, the SMC shall detect a low value on ANA_V12P0_PWRGD. A low value on this signal shall cause the SMC to immediately enter the error state #ERROR_V_12P0 .
- After VREG_GPU_PWRGD is detected, or after tVGPURAMP has expired past asserting VREG_GPU_EN_N, the SMC shall detect a low value on VREG_GPU_PWRGD. A low value on this signal shall cause the SMC to immediately enter the error state ERROR_V_GPUCORE.

[2] *The SMC shall wait at least 2ms and not more than 25ms after detecting the rising edge of ANA_V12P0_PWRGD before assuming that V12P0 is in regulation, and enabling the fault detect for ANA_V12P0_PWRGD.*

- After VREG_CPU_PWRGD is detected, or after tVCPURAMP has expired past asserting VREG_CPU_EN, the SMC shall detect a low value on VREG_CPU_PWRGD. A low value on this signal shall cause the SMC to immediately enter the error state #ERROR_V_CPUCORE.
- After VREG_V3P3_EN_N has been asserted and allowed to become stable (20ms), the SMC shall detect if a backup clock chip is present, and if one is found it shall enable spread spectrum clocking. This happens as follows:
    - The SMC shall attempt an SMBus Block Read
    - If the SMBus Block Read is successful the SMC shall program the ICS clock chip as follows:
        - Perform an SMBus Block Write of size 1 to register 0x2 of the device addressed 0x69 (7-bit address). The data to write is 0xFF.
    - If the low nibble of register 0x6 (logically anded with 0x0F) reads back as 0x08, the SMC shall program the Cypress clock chip as follows:
        - Perform an SMBus Block Write of size 1 to register 0x1 of the device addressed 0x69 (7-bit address). The data to write is 0x83.
        - Perform an SMBus Block Write of size 1 to register 0x4 of the device addressed 0x69 (7-bit address). The data to write is 0xF8.
    - If the low nibble reads back as anything else, or if the read fails, the SMC shall perform no further transactions to the device addressed 0x69 (7-bit address) until it has passed through StandbyInit again. Upon giving up the SMC will immediately enter the error state ERROR_NO_CLOCKCHIP

6.4 Reset Sequence

SMC controls negating reset to the chips in the console.

- The SMC shall maintain a count of the number of attempts it has tried to bring the console out of reset. This count shall be initialized to zero at the start.
- After GPU_RST_N is negated, the SMC shall monitor GPU_RST_DONE before proceeding go the next step in the reset sequence.
    - If GPU_RST_DONE is detected, the SMC shall progress to the next step in the reset negation sequence.
    - If GPU_RST_DONE is not detected within tGPURMAX time, the SMC shall increment the reset attempts counter. The SMC shall log an ErrorGPUResetDone. If the reset attempts counter has reached `MAX_UNRESET_ERRS`, the SMC shall immediately enter the error state ERROR_GPU_RST_DONE. If the reset attempts counter is less than `MAX_UNRESET_ERRS`, the SMC shall run seqReset, and retry seqUnReset without initializing the retry counter.
- After GPU_RST_DONE is asserted, the SMC shall monitor the PCIE_L0_STATUS bits of SFR SFNC to determine when the PCI Express link enters the L0 state.
    - If the SMC detects that the PCI-E link has entered the L0 state, (as defined in the *SB SMC Design* Specification) the SMC shall progress to the next step in the reset negation sequence.
    - If L0 is not detected as set within tLINKTRAIN time, the SMC shall increment the reset attempts counter. The SMC shall log an ErrorLinktrain. If the reset attempts counter has reached `MAX_UNRESET_ERRS`, the SMC shall immediately enter the error state ERROR_NO_PCIE. If the reset attempts counter is less than `MAX_UNRESET_ERRS`, the SMC shall run seqReset, and retry seqUnReset without initializing the retry counter.
- After the PCI-E link has entered the L0 state, the SMC shall negate CPU_RST_N. The SMC shall expect XSS to read the power up cause as a part of XSS's initialization sequence.
    - If the GetPowerUpCause message is received, the SMC transitions to FullOn mode.

- If a GetPowerUpCause message is not received within tCPURMAX of CPU_RST_N being negated, the SMC shall log an ErrorCPUReset. If the reset attempts counter has reached MAX_UNRESET_ERRS, the SMC shall immediately enter the error state ERROR_NO_HANDSHAKE. If the reset attempts counter is less than MAX_UNRESET_ERRS, the SMC shall run seqReset, and retry seqUnReset without initializing the retry counter.

6.5 Error Class Behavior

Error codes listed in the SMC-Detected Error List are grouped into classes. Each class is further explained below. This section is included only for general purpose understanding and may not be accurate. Please refer to the Error.doc, XBox 360 Firmware Requirements.doc, POR Diagram for complete and accurate descriptions.

EC_FATAL

- EC_FATAL is tripped whenever the PWRGD signal of a monitored voltage supply has a falling edge when the supply is enabled. EC_FATAL is also tripped when the SMC cannot read temperature data from Ana. Note that Ana not responding is not necessary a voltage error, but the desired behavior is the same. If Ana cannot be reached, the SMC cannot monitor system temperature, and the console cannot be operated safely. In this case, the console should never be allowed to boot (if detected pre-boot), or should be shut down immediately upon detection.
- When detected all devices shall be put into reset immediately, and all controllable voltages shall be turned off this shall include programming Ana to turn off the thermal sensor and fan op-amps. The SMC shall not wait for the ODD tray to close, to ensure that the power down happens as quickly and safely as possible.
- The ODD tray shall remain non-functional (there will be no power to the tray).
- The console shall remain in this error state indefinitely until a power off event occurs. After a power off event the front panel LED error pattern shall be cleared, and the console shall return to Standby mode.

EC_THERMAL

- When detected, all devices shall be put into reset immediately, and all controllable voltages with the exception of V_12P0 shall be turned off. The SMC shall not wait for the ODD tray to close, to ensure that the power down happens as quickly and safely as possible.
- The fans shall be set to run at their full speed.
- The ODD tray shall remain non-functional (there will be no power to the tray).
- The console shall wait in a Thermal Overload Recovery state for one of the following conditions to occur:
    - any monitored chip temperature continues to exceed its specified maximum for more than five seconds
    - all monitored component temperatures reach the safe turn-off temperature.
    - the maximum thermal recovery time of two minutes has passed
    - any EC_FATAL error occurs. EC_FATAL errors that occur here shall not be reported as EC_FATAL errors, but shall just exit the Thermal Overload Recovery state as the rest of these bullets do.

- Until one of the above conditions is met, power off events shall be ignored. When one of these conditions is met, the console shall finish this shall include programming Ana to turn off the thermal sensor and fan op-amps, and enter an error state similar to the end of EC_FATAL.
- The console shall remain in this error state indefinitely until a power off event occurs. After a power off event the front panel LED error pattern shall be cleared, and the console shall return to Standby mode.

EC_BOOT

- An EC_FATAL_class error causes the console to boot improperly, and is detected by the SMC.
- If the SMC has unreset retries left, the SMC shall run seqReset and seqUnreset when this error occurs.
- If there are no unreset retries left, the SMC shall abort the rest of the unResetSequence, and proceed to FullOn mode. The console shall remain powered.
- The thermal algorithm shall continue to control the fans, as normal.
- The ODD tray shall continue to work as normal.
- When a power-off event occurs, the console shall proceed to Standby mode, closing the ODD tray, and clearing the error pattern.

EC_XSS

- EC_XSS errors are reported to the SMC via the OS module XSS.
- Before the handshake, it is assumed that the error causes the console to boot improperly. It's behavior is:
    - If there are reset retries left, the SMC shall consume a reset retry and attempt to boot the console again. The SMC shall not notify XSS of the impending seqReset, as the SetError received pre-handshake implicity causes the reset.
    - If there are no unreset retries left, the SMC shall treat this error as if it had been reported after the handshake (see below). The SMC shall not finish the unReset sequence if it is interrupted.
- After the handshake:
    - The SMC shall display the error pattern on the front panel.
    - The console shall continue to FullOn mode from GoingFullOn mode, and remain in FullOn mode as normal, with the exception that the front panel LEDs are displaying an error.
    - XSS continues to run, and may display a UEM on the screen.

7 Voltage Resistance List

X801054-009								
PSU Input	Impedance Expected Result	min		nom		max		Location
V_12P0	>100 ohms (charging)	11.4	V	12	V	12.6	V	NE Corner C9A2.1 west side of cap
V_5P0STBY	K ohms	4.75	V	5	V	5.25	V	NE Corner J9A2.1 NW side of connector
Linear VRs		min		nom		max		Location
V_3P3STBY	K ohms	3.22	V	3.3	V	3.39	V	N center U5B1.2 tab of DPAK
V_1P8STBY	>100 ohms	1.748	V	1.8	V	1.851	V	N center U5B2.2 tab of DPAK
V_GPUPCIE	>300 ohms	1.21	V	1.25	V	1.29	V	N of GPU HS U5C1.2 middle leg
V_3P3INTERMEDIATE	>400 ohms	3.22	V	3.3	V	3.39	V	SW corner U1E1.2 tab of DPAK
V_3P3	>400 ohms	3.2	V	3.3	V	3.4	V	SW corner U1F1.4 tab of D2PAK
V_MPORT	>400 ohms	3.22	V	3.3	V	3.39	V	SW corner U1F2.2 tab of DPAK
Switchers		min		nom		max		Location
V_MEM	>30 ohms	1.824	V	1.9	V	1.976	V	SW corner C2F1.1 south side of cap
V_5P0	>500 ohms	4.83	V	5.08	V	5.33	V	SE corner C6G1.1 west side of cap
NOTE: Flip board over so that the fan cutout is still on the North side								
Switchers		min		nom		max		Location
V_CPUCORE	>4 ohms	1	V	1.145	V	1.275	V	W side C7T97.1 SW corner of 0805 cap array
V_GPUCORE	>1 ohm	1.08	V	1.15	V	1.2	V	Middle C5R1.2 north side of cap
Linear VRs		min		nom		max		Location
V_CPUPLL	K ohms	2.09	V	2.2	V	2.31	V	N of CPU U6R1.4 tab of SOT-223
V_SBPCIE	K ohms	1.82	V	1.87	V	1.92	V	NE corner U3P1.4 tab of SOT-223
V_1P8	>100 ohms	1.748	V	1.8	V	1.851	V	E side U2T1.2 tab of DPAK

8 Binary to Hex Conversion Table

Binary	Hex	Binary	Hex	Binary	Hex	Binary	Hex
00000000	00	01000000	40	10000000	80	11000000	C0
00000001	01	01000001	41	10000001	81	11000001	C1
00000010	02	01000010	42	10000010	82	11000010	C2
00000011	03	01000011	43	10000011	83	11000011	C3
00000100	04	01000100	44	10000100	84	11000100	C4
00000101	05	01000101	45	10000101	85	11000101	C5
00000110	06	01000110	46	10000110	86	11000110	C6
00000111	07	01000111	47	10000111	87	11000111	C7
00001000	08	01001000	48	10001000	88	11001000	C8
00001001	09	01001001	49	10001001	89	11001001	C9
00001010	0A	01001010	4A	10001010	8A	11001010	CA
00001011	0B	01001011	4B	10001011	8B	11001011	CB
00001100	0C	01001100	4C	10001100	8C	11001100	CC
00001101	0D	01001101	4D	10001101	8D	11001101	CD
00001110	0E	01001110	4E	10001110	8E	11001110	CE
00001111	0F	01001111	4F	10001111	8F	11001111	CF
00010000	10	01010000	50	10010000	90	11010000	D0
00010001	11	01010001	51	10010001	91	11010001	D1
00010010	12	01010010	52	10010010	92	11010010	D2
00010011	13	01010011	53	10010011	93	11010011	D3
00010100	14	01010100	54	10010100	94	11010100	D4
00010101	15	01010101	55	10010101	95	11010101	D5
00010110	16	01010110	56	10010110	96	11010110	D6
00010111	17	01010111	57	10010111	97	11010111	D7
00011000	18	01011000	58	10011000	98	11011000	D8
00011001	19	01011001	59	10011001	99	11011001	D9
00011010	1A	01011010	5A	10011010	9A	11011010	DA
00011011	1B	01011011	5B	10011011	9B	11011011	DB
00011100	1C	01011100	5C	10011100	9C	11011100	DC
00011101	1D	01011101	5D	10011101	9D	11011101	DD
00011110	1E	01011110	5E	10011110	9E	11011110	DE
00011111	1F	01011111	5F	10011111	9F	11011111	DF
00100000	20	01100000	60	10100000	A0	11100000	E0
00100001	21	01100001	61	10100001	A1	11100001	E1
00100010	22	01100010	62	10100010	A2	11100010	E2
00100011	23	01100011	63	10100011	A3	11100011	E3
00100100	24	01100100	64	10100100	A4	11100100	E4
00100101	25	01100101	65	10100101	A5	11100101	E5
00100110	26	01100110	66	10100110	A6	11100110	E6
00100111	27	01100111	67	10100111	A7	11100111	E7
00101000	28	01101000	68	10101000	A8	11101000	E8
00101001	29	01101001	69	10101001	A9	11101001	E9
00101010	2A	01101010	6A	10101010	AA	11101010	EA
00101011	2B	01101011	6B	10101011	AB	11101011	EB
00101100	2C	01101100	6C	10101100	AC	11101100	EC
00101101	2D	01101101	6D	10101101	AD	11101101	ED
00101110	2E	01101110	6E	10101110	AE	11101110	EE
00101111	2F	01101111	6F	10101111	AF	11101111	EF
00110000	30	01110000	70	10110000	B0	11110000	F0
00110001	31	01110001	71	10110001	B1	11110001	F1
00110010	32	01110010	72	10110010	B2	11110010	F2
00110011	33	01110011	73	10110011	B3	11110011	F3
00110100	34	01110100	74	10110100	B4	11110100	F4
00110101	35	01110101	75	10110101	B5	11110101	F5
00110110	36	01110110	76	10110110	B6	11110110	F6
00110111	37	01110111	77	10110111	B7	11110111	F7
00111000	38	01111000	78	10111000	B8	11111000	F8
00111001	39	01111001	79	10111001	B9	11111001	F9
00111010	3A	01111010	7A	10111010	BA	11111010	FA
00111011	3B	01111011	7B	10111011	BB	11111011	FB
00111100	3C	01111100	7C	10111100	BC	11111100	FC
00111101	3D	01111101	7D	10111101	BD	11111101	FD
00111110	3E	01111110	7E	10111110	BE	11111110	FE
00111111	3F	01111111	7F	10111111	BF	11111111	FF